IN THE SPECIFICATION:

Please delete paragraph [0014].

Please replace paragraphs [0028] to [0035] with the following amended paragraphs:

[0028] ~~figure~~ Figure 1 shows an arrangement of four memory modules which each have nine DRAM memory chips,

[0029] ~~figure~~ Figure 2 shows four modules connected to a common data bus and a conventional control apparatus,

[0030] ~~figure~~ Figure 3 shows four modules connected to a common data bus and a control apparatus in accordance with the invention,

[0031] ~~figures~~ Figures 4a and 4b schematically show the association between the DRAM memory chips and an active group,

[0032] ~~figure~~ Figure 5 schematically shows an arrangement in accordance with the invention with a control apparatus in accordance with the invention,

[0033] ~~figure~~ Figure 6 schematically shows the design of a control apparatus in accordance with the invention, and

[0034] ~~figure~~ Figure 7 shows the use of the signal and data lines in a DRAM module in accordance with the invention by way of example.

[0035] Figure 1 shows 36 very similar semiconductor chips IC1-IC36 which are arranged in groups to form nine respective semiconductor chips IC1-IC36 on four very similar modules M1-M4. In this context, the invention makes provision for any semiconductor chips. In the text below, however, the invention is explained by way of example with reference to memory chips which are arranged as DRAM memory chips,

such as SDR and DDR SDRAMs, on memory modules, "single in-line memory modules" (SIMM) or "dual in-line memory modules" (DIMM). These memory modules, which are known from the area of computers, in particular, are frequently plugged, in the arrangement shown in ~~figure~~ Figure 1, closely together into slots provided for this purpose in a motherboard (not shown in this case) and form the main memory of a computer system. By means of contacts which are preferably arranged along one long edge of a module M1-M4, the modules M1-M4 are connected to the data lines DQ1-DQ72 and also to supply and signal lines in a common data bus DQ (not shown in this case). The figure likewise does not show electrical connecting lines and circuits which are used to connect the memory chips IC1-IC36 to the signal, supply and data lines DQ1-DQ72 in the data bus DQ.

Please replace paragraph [0037] with the following amended paragraph:

[0037] The arrangement shown in ~~figure~~ Figure 1, where semiconductor chips IC1-IC36 are arranged next to one another on modules M1-M4 which are in turn arranged closely together on the motherboard on account of a lack of space, generally promotes little air circulation or convection. This negative effect can be enhanced further by further components situated close to the modules M1-M4 and by the design of the corresponding electronic computer system itself, which means that semiconductor chips IC1-IC36 which are situated in a central region of the arrangement, in particular, are operated in critical temperature ranges. By contrast, the semiconductor chips IC1-IC36 which are situated in an outer region of the arrangement are subject to better air circulation or convection, which means that their operating temperature is usually significantly below the critical temperature. This operating temperature distribution for individual semiconductor chips IC1-IC36 which becomes established along the row arrangements of the semiconductor chips on a module M1-M4 can likewise be seen in the row arrangement of the modules M1-M4. Hence, better air circulation or convection means that the two outer modules M1, M4 will usually have a lower temperature than

the modules M2, M3 inside this row arrangement, where the modules M2, M3 each have immediate neighbors on both sides.

Please replace paragraph [0039] with the following amended paragraph:

[0039] Figure 2 shows a conventional design for a main memory in a computer system. In this case, four modules M1-M4 are connected to the data lines DQ1-DQ72 in a common data bus DQ whose operation is controlled by a control apparatus C. The four modules M1-M4 in ~~figure~~ Figure 1 can be modern SDR or DDR SDRAM memory modules, for example, which, as "DIMMs" ("dual in-line memory modules"), each have eighteen memory chips IC1-IC36 which are respectively distributed over both sides of the module M1-M4 in groups of nine memory chips IC1-IC36. To improve clarity, however, only modules M1-M4 with components on one side are shown in this case. In the example shown, the data bus DQ connecting the four modules M1-M4 to the control apparatus C also has 72 data lines DQ1-DQ72 in addition to control and supply lines. Each of the modules M1-M4 has connecting lines and circuits which are used for connecting the lines in the data bus DQ, which are connected to the contacts on the modules M1-M4, to the memory chips IC1-IC36 arranged on the respective module M1-M4 (not shown in this case).

Please replace paragraph [0040] with the following amended paragraph:

[0040] The conventional design of a modular main memory which is shown in ~~figure~~ Figure 2 has a stipulated organization for the memory chips IC1-IC36. In this case, in the x8 organization of the memory chips which is shown by way of example in this case, each memory chip IC1-IC36 in a module M1-M4 is connected to eight respective data lines DQ1-DQ72 in the data bus DQ. Full use of the 72-bit data bus DQ therefore respectively requires nine of the memory chips IC1-IC36.

Please replace paragraph [0041] with the following amended paragraph:

[0041] As shown by shading in ~~figure~~ Figure 2, a conventional bank organization makes provision for only the memory chips IC1-IC36 in a single module M1-M4 to be respectively activated for data interchange with the data lines DQ1-DQ72 in the data bus DQ. The entire data bus DQ is therefore used up by a respective single module M1-M4.

Please replace paragraph [0043] with the following amended paragraph:

[0043] Figure 3 shows a memory apparatus similar to that in ~~figure~~ Figure 2 having four modules M1-M4 which are connected to a common data bus DQ and each have nine memory chips IC1-IC36 on one side. The modules M1-M4 are connected to a control apparatus C in accordance with the invention by means of the data lines DQ1-DQ72 in the data bus DQ. The inventive control apparatus C has an assessment device S, a selection device E and an activation device A which are shown schematically in ~~figure~~ Figure 3.

Please replace paragraph [0044] with the following amended paragraph:

[0044] To perform data interchange between the modules M1-M4 and the data lines DQ1-DQ72 in the data bus DQ, the inventive method provides a variable bank organization in which a group of memory chips IC1-IC36 is selected on the basis of a prescribed criterion. To this end, the selection unit E selects a particular number of suitable memory chips IC from the total number of memory chips IC1-IC36 on the basis of the prescribed criterion. In this case, the number of selected memory chips IC is determined, depending on the respective form of the memory chips IC1-IC36, such that the total number of data lines DQ1-DQ72 used by the memory chips IC1-IC36 in the group corresponds exactly to the width of the entire data bus DQ. In the case of the x8 organization structure shown in ~~figure~~ Figure 3, with 72 data lines and eight respective

data lines per memory chip IC1-IC36, this corresponds to exactly nine memory chips IC. Since the selection is made independently of module, memory chips IC1-IC36 in all four modules M1-M4 can be selected for the group, in contrast to the firm organization in ~~figure~~ Figure 2. On the other hand, it is also possible to operate using one or more conventionally organized memory banks, e.g. if the power-critical parameter does not exceed a critical value in any of the semiconductor chips IC1-IC36. In this case, a memory bank contains only semiconductor chips IC1-IC36 in a single rank group.

Please replace paragraph [0045] with the following amended paragraph:

[0045] According to the interconnection of the semiconductor chips IC1-IC36 on the modules M1-M4, where the data lines DQ1-DQ72 in the data bus DQ are either firmly associated with a memory chip IC1-IC36 on a module M1-M4 or are allocated individually by a device which is not shown in the present case, the selection device E in the control apparatus C selects the memory chips IC1-IC36 on the basis of or independently of the respective position of the memory chip IC1-IC36 on the corresponding module M1-M4. In the case shown in figures 2 and 3, where the memory chips IC1-IC36 arranged on the modules M1-M4 have a firm association with the data lines DQ1-DQ72 in the data bus DQ, the selection device E in the control apparatus C when selecting a memory chip IC1-IC36 for the group of memory chips IC1-IC36 also needs to take into account the position of the respective memory chip IC1-IC36 on the corresponding module M1-M4, so that no data line DQ1-DQ72 in the data bus DQ is simultaneously assigned to two or more memory chips IC1-IC36 arranged at the same position on the modules M1-M4. As ~~figure~~ Figure 3 shows, each position for a semiconductor chip IC1-IC36 on the modules M1-M4 is therefore selected just for a single module M1-M4. All the selected semiconductor chips IC1-IC36 therefore have different positions on the corresponding modules M1-M4.

Please replace paragraph [0047] with the following amended paragraph:

[0047] A criterion used for selecting a memory chip IC1-IC36 is a power-critical parameter for the respective memory chip IC1-IC36. Preferably, the temperature of the respective memory chip IC1-IC36 is suitable for this, since a central role in the operation of semiconductor chips is attached to this in the face of the drastic power losses which arise when a critical temperature value is exceeded. Furthermore, other power-related parameters for the memory chips IC1-IC36 can also be used as a selection criterion. For the purpose of monitoring the respective power-critical parameter for each memory chip IC1-IC36, the assessment device S is provided, this being in the form of a central device for detecting the temperature of the respective memory chip IC1-IC36 in ~~figure~~ Figure 3 by way of example. In this case, the assessment device S is designed in order to detect the power-related parameters for the memory chips IC1-IC36 on the modules M1-M4 at the present time. In the present case, the temperature of the memory chips IC1-IC36 can preferably be detected using temperature sensors (not shown in this case) which can be arranged on the memory chips IC1-IC36 themselves, on the modules M1-M4 or else outside the modules, as alternatives. The power-related parameter, particularly the temperature, can also be detected centrally, however. To this end, a response for the corresponding memory chips IC1-IC36 is preferably ascertained and evaluated during operation or during a test phase. In the case of the temperature as a selection criterion, responses which are based on electrical properties of the semiconductor circuits in a memory chip IC1-IC36 are also suitable, since these can change with temperature. The temperature of a memory chip IC1-IC36 can thus be ascertained, by way of example, on the basis of an electrical resistance which a prescribed electrically conductive path in the respective memory chip IC1-IC36 has at a particular temperature.

Please replace paragraph [0054] with the following amended paragraph:

[0054] Figures 4a and 4b show a compilation of memory chips to form an optimum bank (Bank1). The association between the memory chips IC1-IC36 and the group

forming the bank is preferably made in this case using CRS indices, which are shown in the present case in the form of a table by way of example. In this context, ~~figure~~ Figure 4a shows an association table for the organization of the memory chips IC from ~~figure~~ Figure 3. In this case, "C" denotes the position of a memory chip IC on a module and "R" denotes the rank, that is to say the order of precedence of the group of memory chips IC which is arranged on one side of the respective module within the arrangement of modules M1-M4.

Please replace paragraph [0056] with the following amended paragraph:

[0056] Figure 5 shows an arrangement in accordance with the invention with a control apparatus C in accordance with the invention, by way of example. The arrangement, which is shown in greatly simplified form in this case, can be a computer system 5, for example. As ~~figure~~ Figure 5 shows by way of example, the inventive control apparatus C also comprises a central processor unit CPU in addition to a memory control device MCU (memory controller unit) for controlling a memory M made up of four modules M1-M4. There is also a buffer store HD which is advantageously in the form of a hard disk. The buffer store HD is used for backing up the content of the memory chips IC1-IC36 on the modules M1-M4 when the memory banks are reorganized in line with the invention. In this context, buffer storage can take place in a similar manner to the inherently known swapping procedures, which involve memory contents being pushed to and fro between the central processor unit CPU, the memory M and the hard disk HD in the computer system 5.

Please replace paragraph [0061] with the following amended paragraph:

[0061] The control apparatus C shown in ~~figure~~ Figure 5 is merely an exemplary embodiment. The selection control device SMU described does not necessarily have to be integrated within the central processor unit CPU. The memory chips IC can also be assessed and selected within the memory control device MCU, for example. It would

likewise be possible to dispense with the buffer store HD for reorganization, depending on the application.

Please replace paragraph [0062] with the following amended paragraph:

[0062] In the text below, two different application scenarios are used to describe how the invention can be used for a computer system 5 shown in greatly simplified form in ~~figure~~ Figure 5.

Please replace paragraph [0071] with the following amended paragraph:

[0071] Figure 6 schematically shows one possible design of a memory control device MCU in accordance with the invention. In this case, the memory control device MCU has, besides components which are known per se, an additional register/latch device RL (Select Bank Reg./Latch) for storing the configuration of the memory banks. In this context, information about the selected memory chips can be stored in the register/latch device RL by the selection control device SMU in the central processor unit CPU in a manner which is shown in figures 4a and 4b, where each memory chip is identified by means of an individual CRS index. If data access is taking place, this information can be read by a sequencer (CMD + Timing Logic) which activates the corresponding memory chips IC on the basis of their CRS indices. To this end, as indicated in ~~figure~~ Figure 6, additional control lines CRS0-8 can be provided between the sequencer and the individual memory chips IC, these being used to actuate the corresponding memory chips IC.

Please replace the Abstract with the following amended Abstract:

The invention relates to a method for operating semiconductor chips, particularly memory chips, which are arranged in groups on modules which are connected to a common data bus ~~where~~ wherein each semiconductor chip on each module is connected to at least one data line in the common data bus ~~having~~ comprising the following method steps:

a) selecting a group of semiconductor chips ~~is selected~~ from the semiconductor chips arranged on the modules based on ~~the basis of~~ a prescribed selection criterion independently of module, the selected group of semiconductor chips using [[the]] data lines in the common data bus over the entire bus width;

b) activating the semiconductor chips in the selected group ~~are activated~~; and

c) performing data interchange ~~is performed~~ between the data lines in the common data bus and the selected group of semiconductor chips.